Fuji Switching Power Supply Control IC

Green Mode PWM IC

FA5558/87/88/89
FA5581/82/83/84

Application Note

December-2008
Fuji Electric Device Technology Co., Ltd.

Caution

1. The contents of this note (Product Specification, Characteristics, Data, Materials, and Structure etc.) were prepared in December 2008.
   The contents will subject to change without notice due to product specification change or some other reasons. In case of using the products stated in this document, the latest product specification shall be provided and the data shall be checked.

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4. Products described in this note are manufactured and intended to be used in the following electronic devices and electric devices in which ordinary reliability is required:
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   - Machine tool - Audio Visual equipment - Home appliance - Personal equipment
   - Industrial robot etc.

5. Customers who are going to use our products in the following high reliable equipments shall contact us surely and obtain our consent in advance. In case when our products are used in the following equipment, suitable measures for keeping safety such as a back-up-system for malfunction of the equipment shall be taken even if Fuji Electric semiconductor products break down:
   - Transportation equipment (in-vehicle, in-ship etc.) - Communication equipment for trunk line
   - Traffic signal equipment - Gas leak detector and gas shutoff equipment
   - Disaster prevention/Security equipment - Various equipment for the safety.

6. Products described in this note shall not be used in the following equipments that require extremely high reliability:
   - Space equipment - Aircraft equipment - Atomic energy control equipment
   - Undersea communication equipment - Medical equipment.

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Caution)

- The contents of this note subject to change without notice due to improvement.
- The application examples or the parts constants in this note are shown to help your design. Variation of parts and service condition are not fully taken into account. Before use, a design with due consideration for these variations and conditions shall be conducted.

1. Overview

FA5558/87/88/89/81/82/83/84 is a current mode type switching power supply control IC possible to drive a power MOSFET directly. Despite of a small package with 8 pins, it has a lot of functions and it is best suited for power saving at the light load and decreasing external parts. Moreover it enables to realize a reduced space and a high cost-performance power supply.

2. Features

- Excellent Power Saving by lowering the oscillation frequency depending on the load at light load.
- Low power consumption by a built-in 500V high voltage startup circuit.
- Current Minus detection. Power Saving of the revision of the input voltage of OLP.
- Overload protection function(OLP) is built in it. Auto Recovery type or Timer Latch type.
- Brown-In/Out Function without additional external components.
- VCC Over-Voltage Protection function(OVP). (Vcc=26V).
- VCC Under-Voltage Lock-Out function (UVLO). (Vcc=18V/9.8V)
- Minimum ON width is replaced and restrains transient leaping up of the drain voltage of the MOSFET.
- Latch pin for an external signal: Over Temperature Protection, Over Voltage Protection etc.
- External MOSFET driving suitable for Power Supply up to 200W: -1.0A(sink),/+0.5A(source)
- Soft Start function.

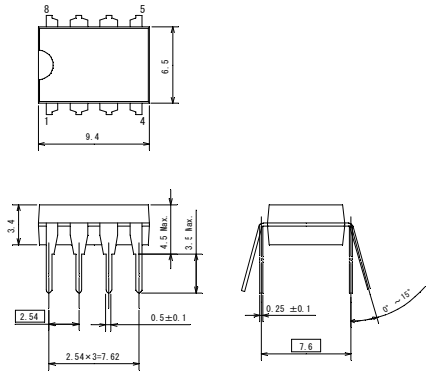
Function list

Type	Switching frequency(Fosc)	OLP(OverLoad Protection) Type	OLP Delay time	OLP restart time	VthIS1(Voltage for current detection)
FA5558N *1	60kHz	Auto Recovery	70ms	1530ms	-0.95V
FA5587N	60kHz	Latch	70ms	-	-0.95V
FA5588N *1	100kHz	Auto Recovery	70ms	1530ms	-0.95V
FA5589N *1	100kHz	Latch	70ms	-	-0.95V
FA5581N *1	100kHz	Latch	70ms	-	-0.45V
FA5582N *1	100kHz	Auto Recovery	70ms	1530ms	-0.45V
FA5583N *1	60kHz	Latch	70ms	-	-0.45V
FA5584N *1	60kHz	Auto Recovery	70ms	1530ms	-0.45V

*1: During development

3. Outline drawing

DIP-8



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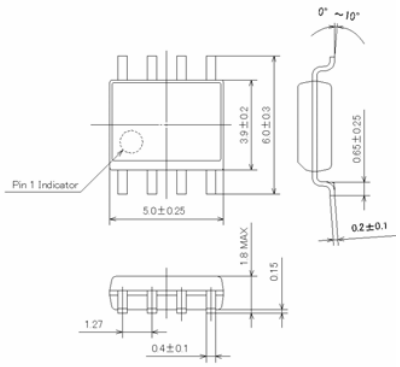
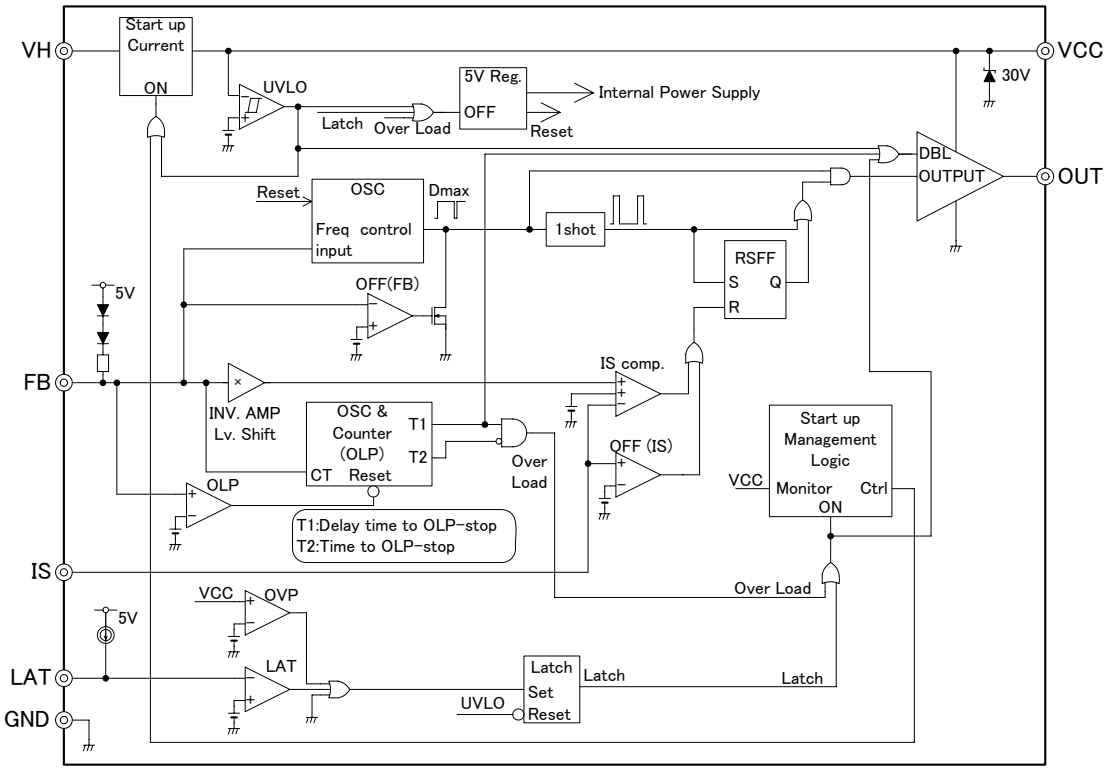
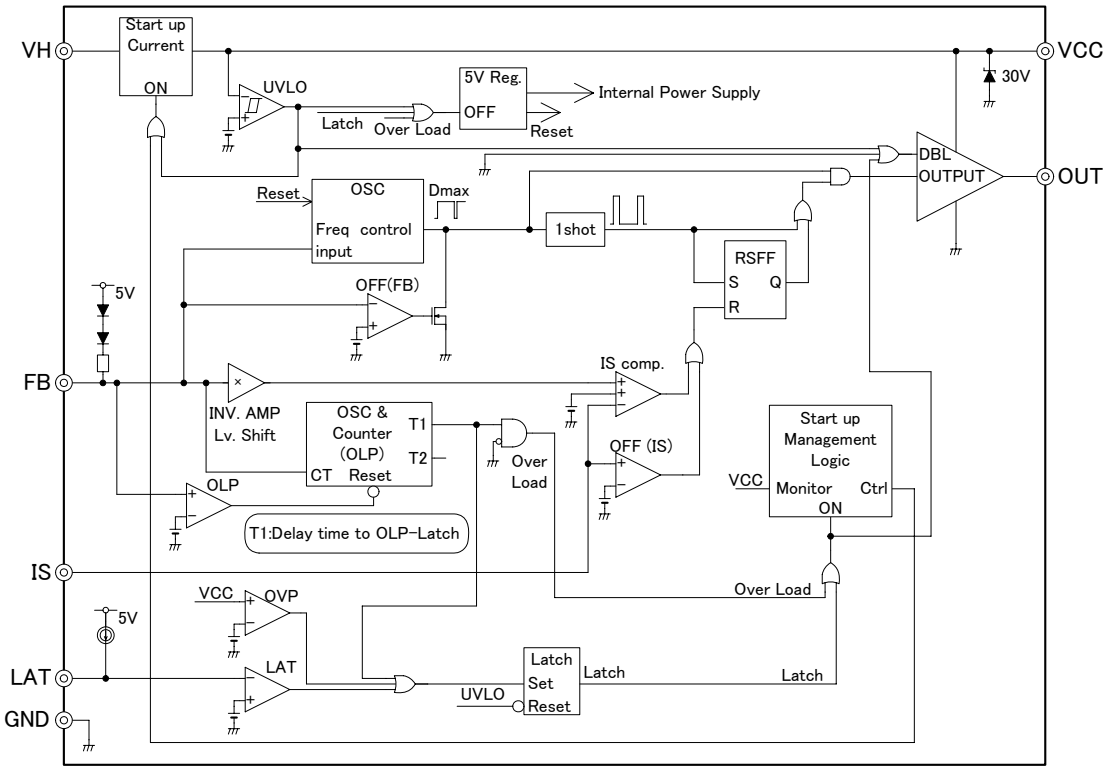


4. Block diagram

FA5558/88/82/84 (Overload Protection : Auto-Recovery type)

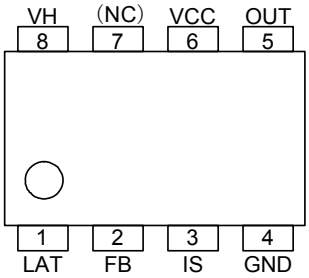


FA5587/89/81/83 (Overload Protection : Timer Latch type)



5. Functional description of pins

Pin No.	Pin Name	Pin function
1	LAT	External latch signal input. Soft start.
2	FB	Feed back input. Light load and OLP detect
3	IS	Current sense
4	GND	Ground
5	OUT	Driver Output
6	VCC	Power supply
7	(NC)	(No Connection)
8	VH	High voltage input. Brown-out detect



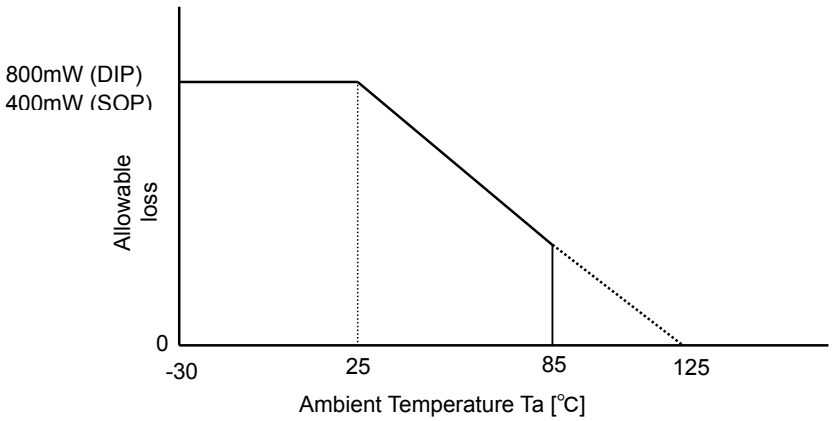
6. Rating & characteristics

* "+" shows sink and "–" shows source in current prescription.

(1) Absolute maximum rating

Item	Symbol	Rating	Unit
Power supply voltage	VCC	28	V
OUT pin output peak current	Ioh	-0.5	A
	Iol	+1.0	A
OUT pin voltage	VOUT	-0.3 to Vcc+0.3	V
FB pin voltage	VFB	-0.3 to 5.0	V
IS pin voltage	VIS	-2.0 to 5.0	V
LAT pin voltage	VLAT	-0.3 to 5.0	V
VH pin input voltage	VVH	-0.3 to 500	V
Total loss (Ta = 25℃)	Pd	800 (DIP-8)	mW
		400 (SOP-8)	mW
Junction temperature in operation	Tj	-30 to 125	℃
Storage temperature	Tstg	-40 to 150	℃

○Allowable loss reduction characteristics



(2) Recommended operating condition

Item		Symbol	MIN	TYP	MAX	Unit
VCC Power supply voltage		VCC	11	18	22	V
High input voltage	Direct voltage	VVH(DC)	100		450	V(DC)
	Half-wave rectification	VVH(AC1)	80		288	V(AC)
	Full-wave rectification	VVH(AC2)	80		288	V(AC)
VH pin Resistance		RVH	2	---	10	k ohm
LAT pin capacity		CLAT	0.22	1.0	2.2	uF
VCC pin capacity		CVCC	10	33	100	uF
Operating ambient temperature		Ta	-30		85	℃

(3) Electric characteristics (Tj=25℃, Vcc=18V, unless otherwise specified)

Switching oscillator section (FB pin)

Item	Symbol	Conditions		MIN	TYP	MAX	Unit
Oscillation frequency	Fosc	VFB=3V	FA5558/87 FA5583/84	54	60	66	kHz
			FA5588/89 FA5581/82	(90)	100	(110)	kHz
Voltage stability	Fdv	VCC：11V to 24V		-2	—	+2	%
Temperature stability *1	Fdt	Tj= -30 to 125℃		-5	—	+5	%
FB pin threshold voltage for light load mode	Vfbm			0.95	1.15	1.35	V
Oscillation frequency reduction ratio	kf	Δf/ΔVfb	FA5558/87 FA5583/84	200	240	280	kHz/V
			FA5588/89 FA5581/82	(340)	390	(440)	kHz/V
Minimum oscillation frequency	Fmin			0.22	0.34	0.50	kHz

External latch-off section (LAT pin)

Item	Symbol	Conditions		MIN	TYP	MAX	Unit
Source current of LAT pin	Ilat	LAT=1.1V Charge period	FA5558 FA5588/89 FA5581/82 FA5583/84	-80	-70	-60	uA
			FA5587	-77.7	-70	-62.3	uA
Latch-off level	VthLAT			1.00	1.05	1.10	V
Latch-off delay timer *1	TdLAT			50	65	80	us

Pulse width modulation section (FB pin)

Item	Symbol	Conditions	MIN	TYP	MAX	Unit
Maximum duty cycle	Dmax	FB=4.5V	75	80	85	%
Minimum duty cycle	Dmin	FB=0V	—	—	0	%
Input threshold voltage	VthFB0	DUTY=0%	340	400	460	mV
FB pin source current	Ifb0	VFB=0V	-300	-250	-200	uA

Over load protection circuit section (FB pin)

Item	Symbol	Conditions		MIN	TYP	MAX	Unit
Over load detection threshold voltage *1	VthOLP			2.5	3.0	3.5	V
Over load protection Delay time	TdOLP	VFB=4V		60	70	80	ms
Waiting time of auto restart *1	TdOLP2	VFB=4V	FA5558/88 FA5582/84	(1300)	1530	(1760)	ms

Current sense section (IS pin)

Item	Symbol	Conditions		MIN	TYP	MAX	Unit
Voltage gain	AvIS	ΔVFB/ΔVIS	FA5558/87 FA5588/89	-2.7	-2.3	-1.9	V/V
			FA5581/82 FA5583/84	(-5.4)	-4.6	(-3.8)	V/V
Maximum threshold voltage (Current sense)	VthIS1	VFB=3V	FA5558/87 FA5588/89	-1.05	-0.95	-0.85	V
			FA5581/82 FA5583/84	(-0.52)	-0.45	(-0.38)	V
Input bias current	IIS	VIS=0V		-50	-40	-30	uA
Minimum ON pulse width	Tmin	Steady		950	1250	1500	ns
		Start/Restart		180	280	380	ns
Delay to output *1	TpdIS	Tj=25℃		50	200	300	ns

VCC circuit section (VCC pin)

Item	Symbol	Conditions	MIN	TYP	MAX	Unit
Start-up threshold voltage	VCCon		16	18	20	V
Shutdown threshold voltage	VCCoff		8.8	9.8	10.8	V
Hysteresis width	Vhys		6.8	8.2	9.6	V
VCC over-voltage protection threshold voltage	Vthovp	Tj=25℃	25	26	27	V

Output circuit section (OUT pin)

Item	Symbol	Conditions	MIN	TYP	MAX	Unit
Low output voltage	VOL	IOL=100mA, VCC=18V	0.5	1.0	2.0	V
High output voltage *1	VOH	IOH= -100mA, VCC=18V	(14.5)	(16)	17	V
Rise time *1	tr	CL=1000pF, Tj=25℃	30	60	100	ns
Fall time *1	tf	CL=1000pF , Tj=25℃	20	40	70	ns

High-voltage input section (VH pin、VCC pin)

Item	Symbol	Conditions	MIN	TYP	MAX	Unit
Input Current of VH pin	IHrun	VH=450V, VCC > VCCon	90	130	170	uA
	IHstb	VH =120V, VCC =0V	3.5	6.2	9.0	mA
Threshold voltage level at brown-out (VH pin)	VthBO	VH pin : Decreasing	92	99	106	V
Threshold voltage level at Brown-in (VH pin)	VthBI	VH pin : Increasing	97	104	111	V
Brown-out Delay time	TpdBO		45	50	55	ms
VCC voltage at Brown - out	VCCBH	VH=80V, Upper level	17	18	19	V
	VCCBL	VH=80V, Lower level	14.5	15.5	16.5	V
VCC voltage at Latch	VCCLHH	VH =120V, 1 time clamp	13	14.5	16	V
	VCCLH	VH=120V, Upper level	12	13	14	V
	VCCLL	VH =120V, Lower level	11	12	13	V
Charge current for VCC pin	Ipre1	VCC =16V, VH =120V	-8	-4.9	-2	mA
	Ipre2	VCC =11V,VH =120V at Latch	-8.2	-5.3	-2.8	mA

Power supply current (VCC pin)

Item	Symbol	Conditions		MIN	TYP	MAX	Unit
Operating-state supply current	ICCop1	Duty cycle=Dmax VFB=2V, OUT=No Load	FA5558/87 FA5583/84	1.0	1.3	1.6	mA
			FA5588/89 FA5581/82	(1.2)	(1.5)	(1.8)	mA
	ICCop2	Duty cycle=0% VFB=0V	FA5558/87 FA5583/84	0.95	1.25	1.55	mA
			FA5588/89 FA5581/82	(1.15)	1.45	(1.75)	mA
Supply current at Brownout	ICCbo	FB=open,VH=80 V, VCC=14.5V	FA5558/87 FA5583/84	600	800	1100	uA
			FA5588/89 FA5581/82	(650)	850	(1150)	uA
Latch mode supply current	ICClat	FB=open, VCC=11V	FA5558/87 FA5583/84	600	800	1100	uA
			FA5588/89 FA5581/82	(650)	850	(1150)	uA
VCC pin zenner clamp voltage	VCCzd	OUT：No Load Icc=2mA		28	30	34	V

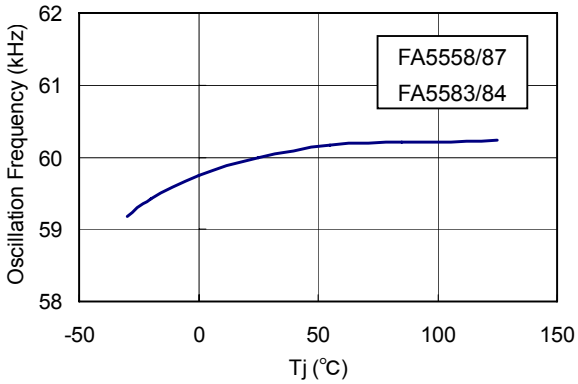
*1:This parameter is not 100% tested in production but guaranteed by design.

It doesn't guarantee the column of '-' to have been specified.

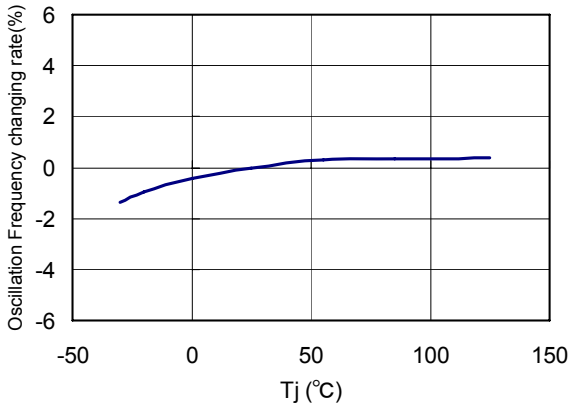
7. Characteristics curve

- In case nothing is specified otherwise: Ta=25℃, VCC＝18V
- "+" shows sink and "–" shows source in current prescription.
- Data written here show the typical characteristics of the IC and do not guarantee the characteristics.

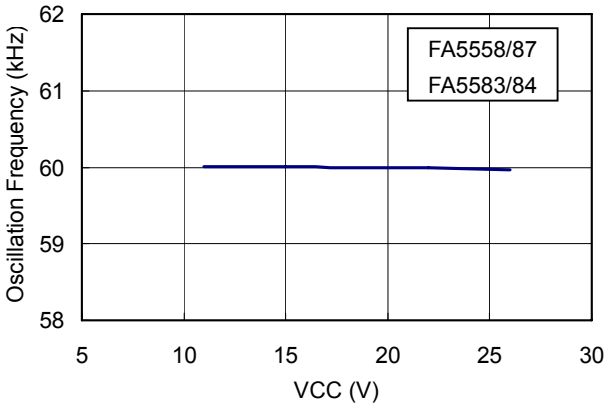
Oscillation Frequency (Fosc)
vs. Junction temperature(Tj)



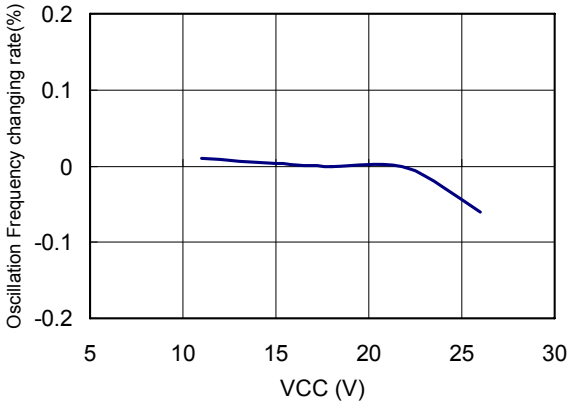
Oscillation Frequency (FOSC) changing rate
vs. Junction temperature(Tj)



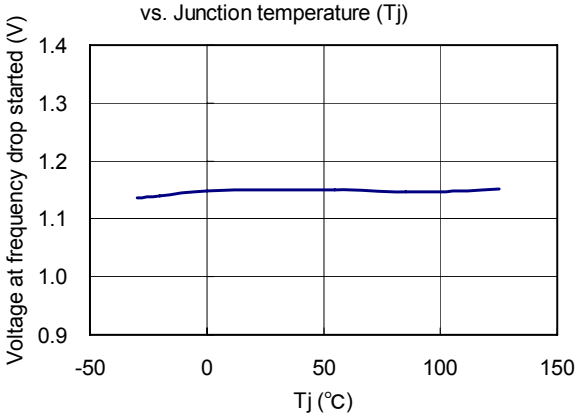
Oscillation Frequency (Fosc)
vs. Power supply voltage (VCC)



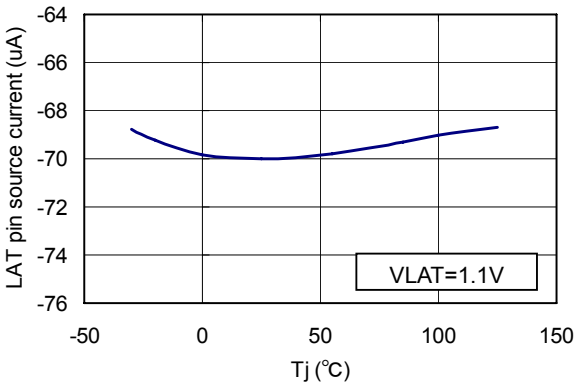
Oscillation Frequency (Fosc) changing rate
vs. Power supply voltage (VCC)



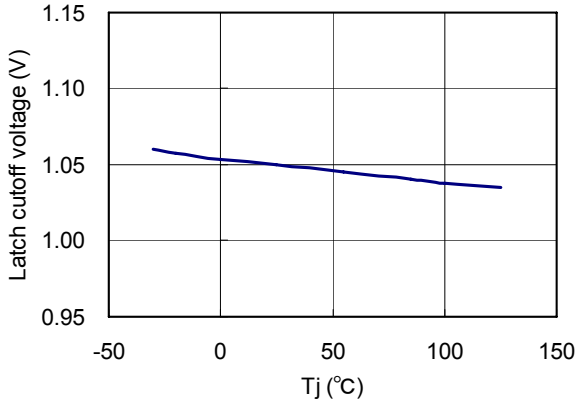
FB pin voltage at frequency drop started (Vfbm)
vs. Junction temperature (Tj)



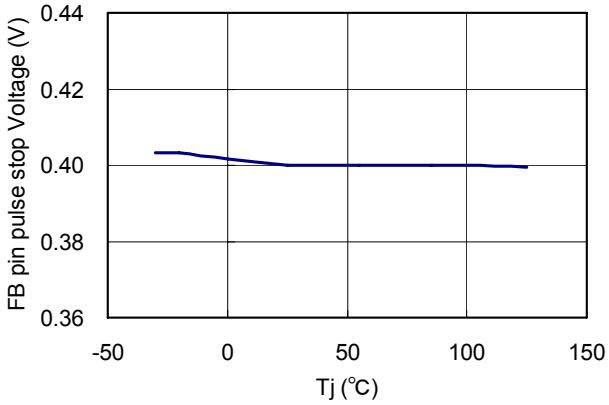
LAT pin source current (Ilat)
vs. Junction temperature (Tj)



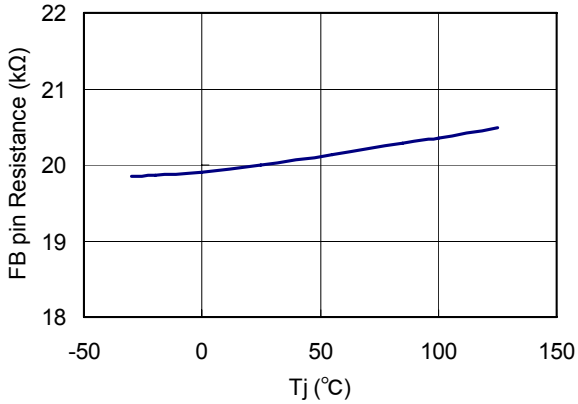
Latch cutoff threshold voltage (VthLAT)
vs. Junction temperature (Tj)



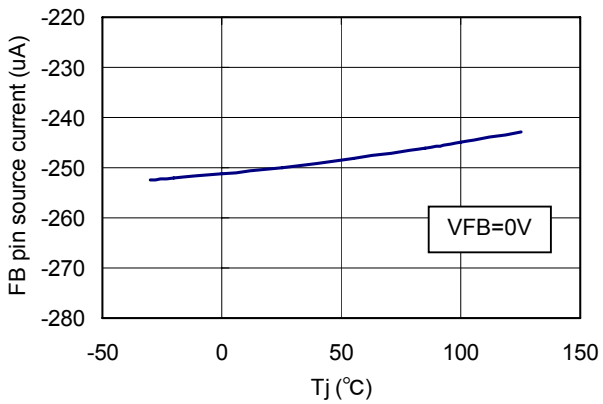
Output shutdown threshold voltage (VthFB0)
vs. Junction temperature



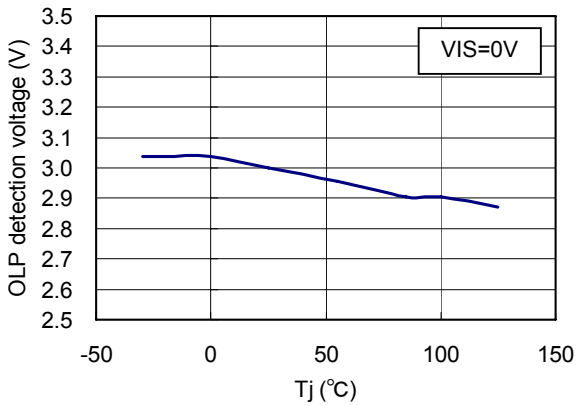
FB pin input resistance (Rfb)
vs. Junction temprature (Tj)



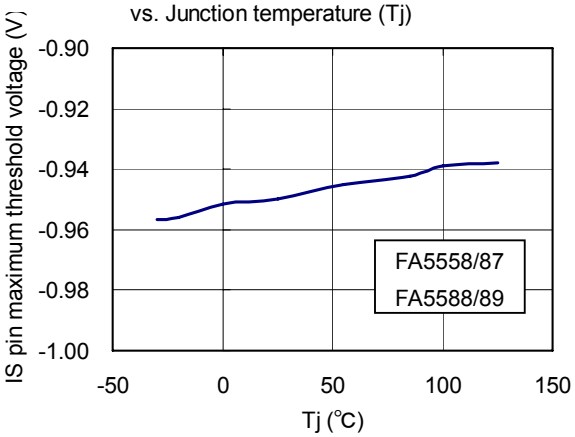
FB pin source current (Ifb0)
vs. Junction temperature (Tj)



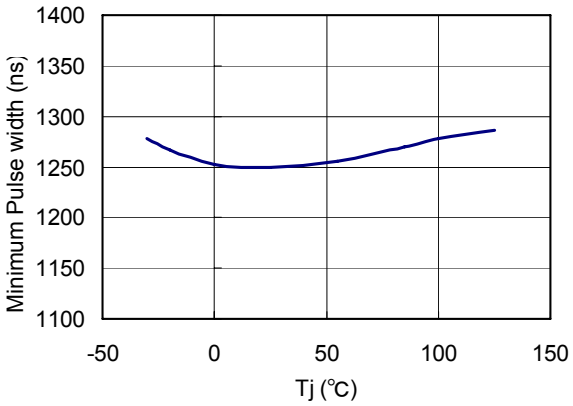
OLP detection voltage (VthOLP)
vs. Junction temperature (Tj)



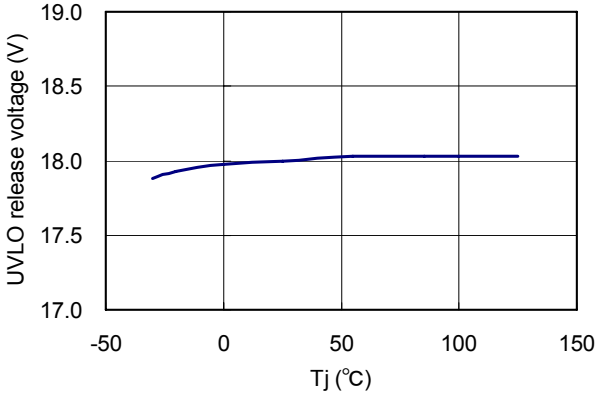
Current sense maximum input threshold voltage(VthIS)
vs. Junction temperature (Tj)



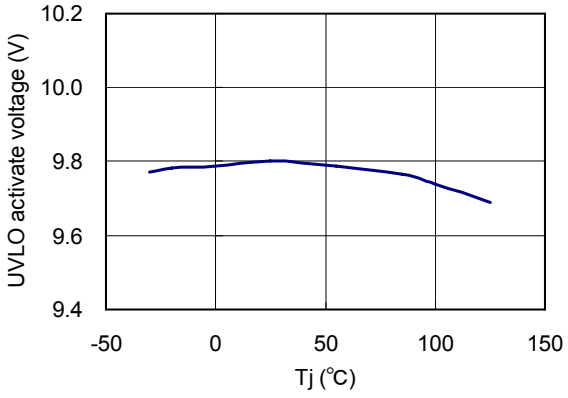
Minimum ON width (Tmin)
vs. Junction tmperature (Tj)



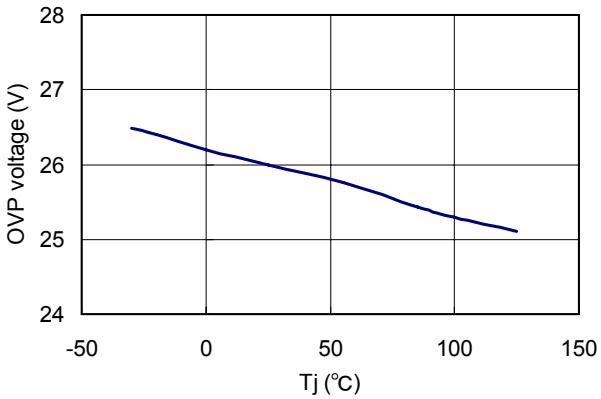
UVLO release threshold voltage (VCCon)
vs. Junction temperature (Tj)



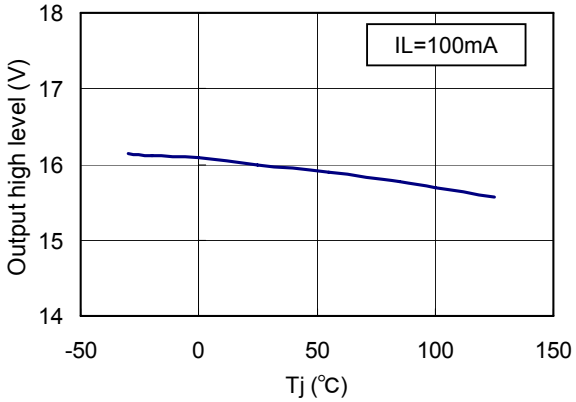
UVLO activate threshold voltage (VCCoff)
vs. Junction temperature (Tj)



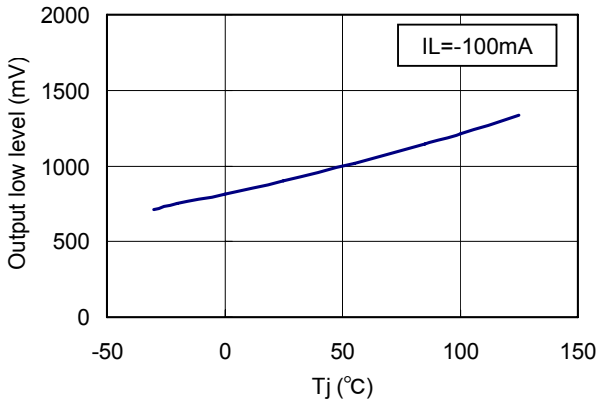
Overvoltage threshold voltage (VthOVP)
vs. Junction tmperature (Tj)



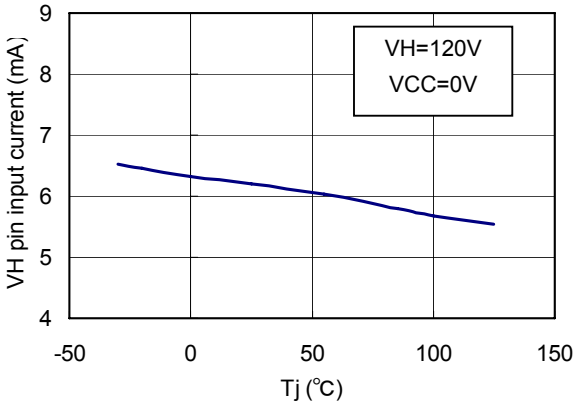
Output voltage high level (VOH)
vs. Junction tmperature (Tj)



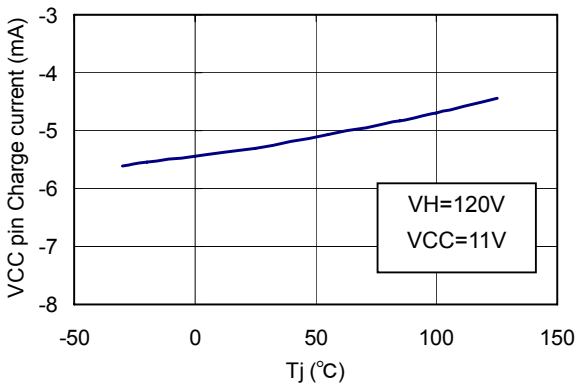
Output voltage low level (VOL)
vs. Junction temperature (Tj)

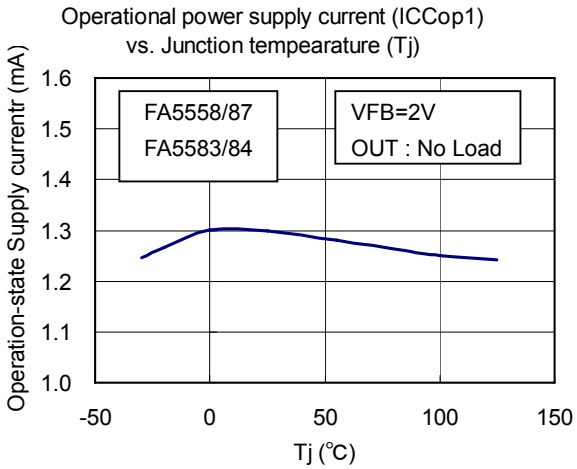


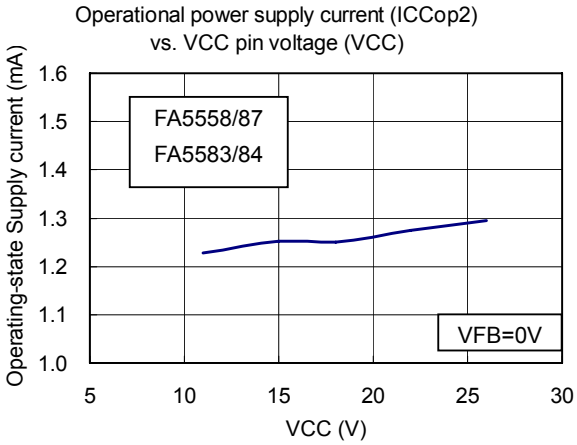
VH pin input current (IHstb)
vs. Junction temperature (Tj)

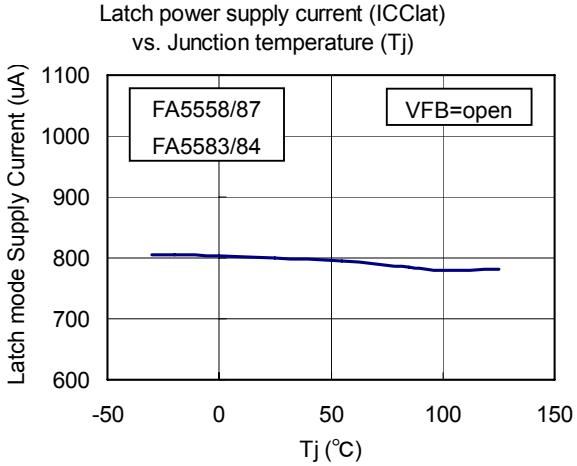


VCC pin capacitance charge current (Ipre2)
vs. Junction temperature (Tj)









8. Operation of each block

(1) Startup circuit

The IC integrates a startup circuit having withstand voltage of 500V to achieve low power consumption.
Fig.1 to Fig.3 show connections.
Turning on the power, capacitor C2 connected to the VCC terminal is charged and the voltage increases due to the current fed from the startup circuit to the VCC terminal. If the ON threshold voltage (Vcc = 18V typ) of the under-voltage lockout circuit (UVLO) is exceeded, the power for internal operation is turned on, and the IC starts operating.
The current supplied from the VH terminal to the VCC terminal is approximately 6mA when VCC = 0V. As the VCC voltage increases, the supply current decreases and reaches 4.9mA at the startup voltage.
After IC operation is started, the startup circuit is shut down to minimize power loss. The current flowing into the VH terminal is 130μA (typ) at VH = 450Vdc.
A resistor, RVH (2k to 10kΩ), is connected in series to the VH terminal to prevent the IC from being damaged by the surge voltage of the AC line.

Fig.1 shows a typical connection where the VH terminal is connected to the half-wave rectifier circuit of AC input voltage.
The startup time of this connection is the longest in 3 types of connection. However, if AC input voltage is shut down after the IC enters the latch mode, the supply of current from the VH terminal is interrupted by overload or overvoltage protection, which allows the latch mode to be reset in a time as short as several seconds.

Fig.2 shows the connection where the VH terminal is connected to the full-wave rectifier circuit of AC input voltage. The startup time of this connection is approximately half of the connection shown in Fig.1, and its latch mode reset time can be made as short as that of connection shown in Fig.1 by interrupting the AC input voltage.

Fig.3 shows the connection where the VH terminal is connected to the back of rectification and smoothing of AC input voltage. The startup time of this connection is the shortest in 3 types. In this connection, however, even if the AC input voltage is shut down after the IC enters the latch mode, the voltage charged in C1 is kept impressed to the VH terminal, requiring much time for the latch mode to be reset. It takes approximately several minutes to reset the latch mode, although the time varies depending on conditions.

After the startup, the IC goes into switching operation, and is operated with the power supplied from the auxiliary winding. While the brownout function is working in a state in which the AC input voltage is low, the VCC voltage is kept within the 15.5V to 18V (typ) range by the ON/OFF control of the startup circuit. If the overload or overvoltage protection is actuated, causing the IC to enter the latch mode, the one time clamp circuit discharges the VCC voltage immediately down to 14.5V (typ). This function interrupts the AC input voltage and shortens the latch mode reset (by the UVLO reset function) time. Then the startup circuit is subjected to ON/OFF control to maintain the VCC voltage within the 12V to 13V (typ) range. The VCC voltage of the auto recovery type is maintained within the 15.5V to 18V (typ) range by the ON/OFF control of the startup circuit during the auto reset wait time after the overload shutdown.

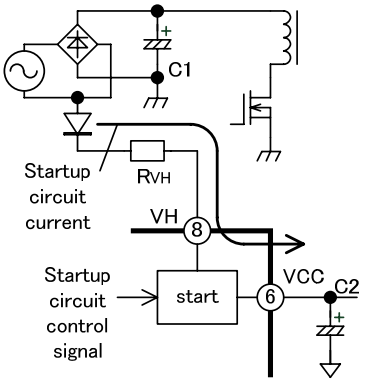


Fig.1 Startup circuit 1 (Half-wave)

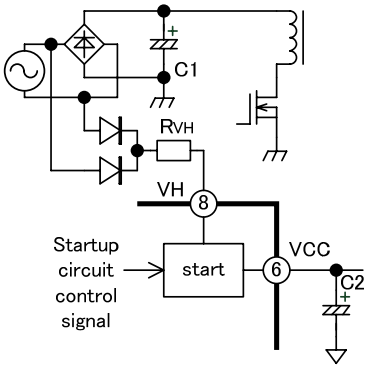


Fig.2 Startup circuit 2 (Full-wave)

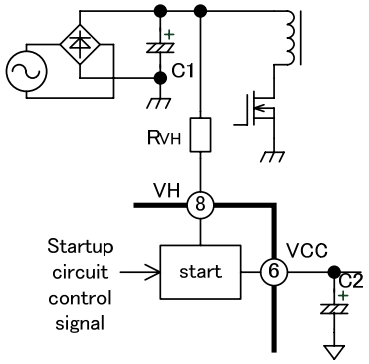


Fig.3 Startup circuit 3 (Rectification)

(2) Oscillator

This oscillator is used to determine the switching frequency. The switching frequency in the normal operation mode is set to 60kHz (typ) or 100kHz (typ) within the IC.

To minimize the loss of power in the standby state, this IC is equipped with a function of automatically decreasing the switching frequency under light load.

When the FB terminal voltage decreases down to 1.15V (typ) or lower under light load, the frequency decreases almost linearly proportional to the FB terminal voltage.(See Fig.4) The minimum frequency, Fmin, has been set to 0.34kHz (typ).

When the load further decreases and thus the FB terminal voltage decreases down to 0.4V (typ) or lower, the switching is stopped. (See one-shot circuit.)

In addition to trigger signals for determining switching frequency, the oscillator generates pulse signals for determining the maximum duty cycle and ramp signals for performing slope compensation.

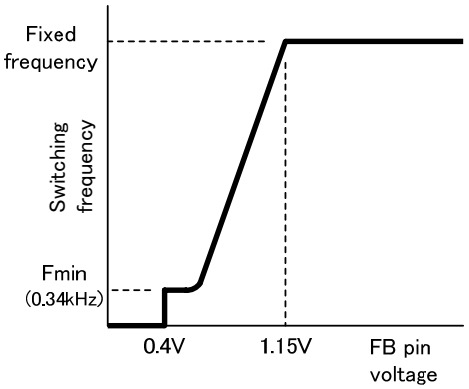


Fig. 4 Oscillation frequency

(3) Current comparator and PWM latch circuit

The IC performs current mode control. Fig.5 shows a circuit block for basic operations, and Fig.6 shows a timing chart.

The polarity of the current detection voltage of the IS terminal is negative. The GND of the IC is connected between the current detection resistor Rs and the MOSFET. (See Fig.5)

A trigger signal having the switching frequency that is output from the oscillator is input to the PWM latch (F.F.) through the one-shot circuit as a set signal. Then the output of the PWM latch as well as the OUT terminal voltage reaches the High state.

On the other hand, the current comparator (IS comp.) monitors the MOSFET current, and if the threshold voltage is reached, a reset signal is output. When a reset signal is input, the output of PWM latch (F.F.) as well as the OUT terminal voltage reaches the Low state.

The ON pulse width of the OUT terminal is thus controlled with the threshold voltage of the current comparator (IS comp.).

The output is controlled by changing the threshold voltage of this IS comp. with feedback signals.

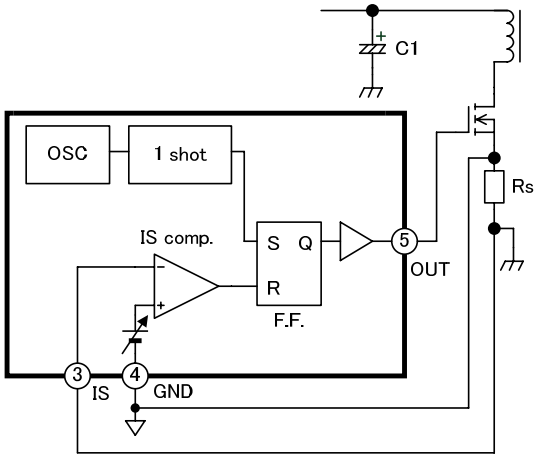


Fig. 5 Current mode basic operation circuit block

As shown in Fig.7, the FB terminal voltage is level-shifted by a reverse amplifier and input into the current comparator (IS comp.) as the threshold voltage. In addition, -0.95V (typ) or -0.45V (typ) reference voltage is input inside the IC to regulate the maximum input threshold voltage of the IS terminal, VthIS1 (overcurrent control threshold).

The reverse amplifier output or the maximum IS terminal input threshold voltage, VthIS1, whichever is higher, is given precedence as the IS terminal threshold voltage.

(Example: When the output of the reverse amplifier is -0.5V in a product whose maximum threshold voltage of the IS terminal, VthIS1, is -0.95V, the output of the reverse amplifier is given precedence and thus the current comparator is reversed when the IS terminal voltage reaches -0.5V.)

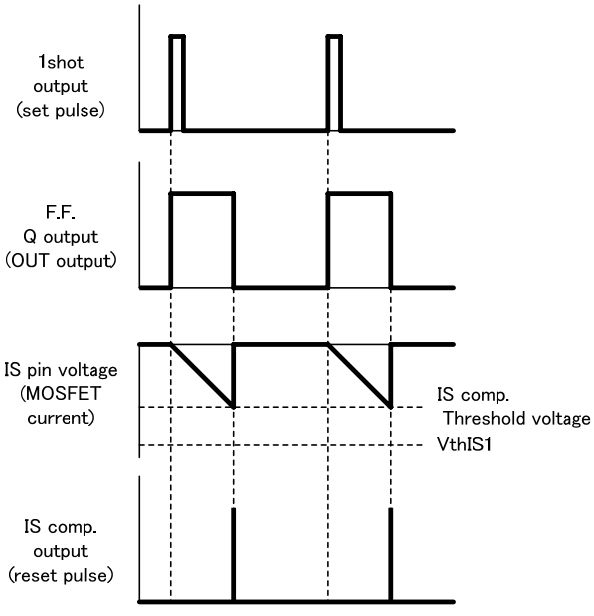


Fig. 6. Current mode basic operating timing chart

In normal operation, the output voltage of the power supply is maintained constant by changing the threshold voltage of the current comparator via the FB terminal voltage.
When the output voltage decreases, the feedback circuit increases the FB voltage to allow the threshold voltage of the current comparator to scale out to Low, thus increasing the MOSFET current.
The maximum input threshold voltage of the IS terminal, VthIS1 (-0.95V or -0.45V typ) controls the maximum current of the MOSFET. If the FB terminal voltage increases under overload, the output of the reverse amplifier scales out to Low, decreasing down to lower than VthIS1. The threshold voltage of the IS terminal is thus controlled not to exceed VthIS1.

The oscillator outputs pulses for determining the maximum duty cycle. Using these pulses, the maximum duty cycle has been set to 80% (typ).

(4) One shot circuit (minimum ON width)

When the MOSFET is turned on, a surge current is generated due to discharge corresponding to the capacitance of the main circuit and gate drive current. If this surge current reaches the IS terminal threshold voltage, the current comparator output is reversed, and consequently normal pulses may not be generated from the OUT terminal.
To avoid this phenomenon, a minimum ON width of OUT terminal output is set within the one-shot circuit block of the IC.
If a trigger signal having the switching frequency is input from the oscillator, a pulse having a specific width is output as a PWM latch (F.F.) set signal.
Since the set signal has priority over the input signal of the PWM latch, the output of the PWM latch (F.F.) is not reversed while the set signal from the one-shot circuit is being input, even if a reset signal is input from the current comparator (IS comp.) (See Fig.5)
As a result, the input to the IS terminal is kept invalid for the specified period of time immediately after the output pulse is generated from the OUT terminal (minimum ON width), and made not to respond to the surge current at turn-on. (See Fig.8)
This minimum ON width function eliminates the need of a noise filter for the IS terminal in principle.

The minimum ON width is usually set to 1250ns (typ) in normal operations, and to 280ns (typ) at startup or rebooting to prevent the transient MOSFET drain voltage from surging.

In addition, an exclusive comparator is integrated to keep the output pulse at zero under no load. (See Fig.9)
This comparator reverses its output when the FB terminal voltage decreases down to 400mV (typ), preventing a set pulse to be input to the PWM latch (F.F.). The output is thus maintained in Low state and switching is stopped.

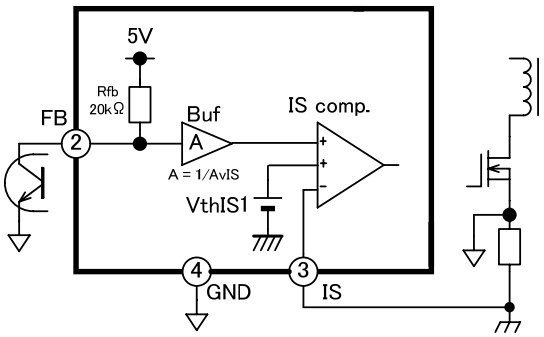


Fig.7 Current comparator

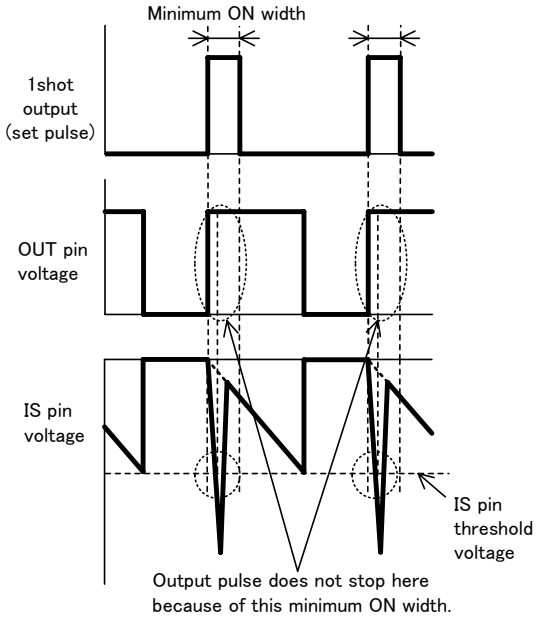


Fig.8 Minimum ON width

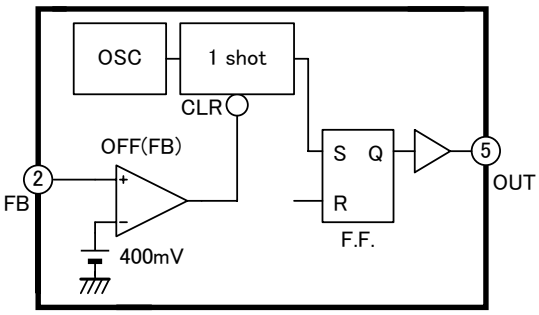


Fig.9 Output shutdown function of FB pin

(5) Overload protection circuit (auto reset type)

Detecting overload, the overload protection (OLP) circuit stops switching in case overload is continued for a specified period of time (70ms typ) to protect the circuit.
Overload detection is performed based on the FB terminal voltage.
Fig.10 is a conceptual diagram of the operation.
Fig.11 shows a circuit block, and Fig.12 shows the protection operation timing chart, of the auto reset type.

The overload protection is actuated when FB terminal voltage processed into a signal is detected with the OLP comparator, based on the overload delay time TdOLP (70ms typ), which is the period from the overload detection with the built-in OLP timer to switching pulse stop, and the auto reset wait time TdOLP2 (1530ms typ), which is the period from switching stop to switching restart. These periods are specified within the IC.

When the output current increases and the FB terminal voltage increases up to VthOLP (3.0V typ), overload is detected. Since the IS terminal voltage is equivalent to the maximum input threshold voltage VthIS1 (-0.95V or -0.45V typ) at this time, the MOSFET current is limited, and the output voltage is no longer maintained.
As soon as the overload is detected, the OLP timer starts counting the delay time up to the stop of the switching pulse.
When specified overload protection delay time TdOLP (70ms typ) has elapsed, the switching pulse output is stopped. If overload is reset and the FB voltage decreases down to VthOLP (3.0V typ) before the overload protection delay time expires, switching continues.

When switching is stopped, the OLP timer counts the auto reset wait time TdOLP2 (1530ms typ).
The startup circuit is kept under the ON/OFF control while switching is suspended, and the VCC voltage is kept within the 15.5V to 18V (typ) range.
When auto reset wait time TdOLP2 has elapsed, the switching pulse is output for rebooting.

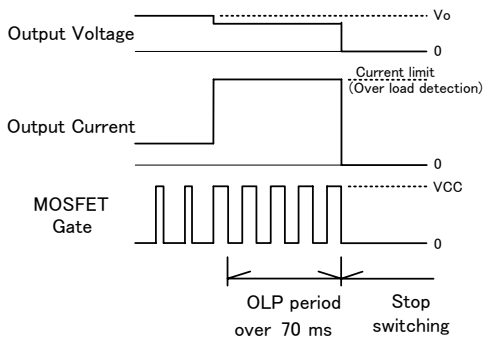


Fig. 10 Conceptual diagram of overload protection operation

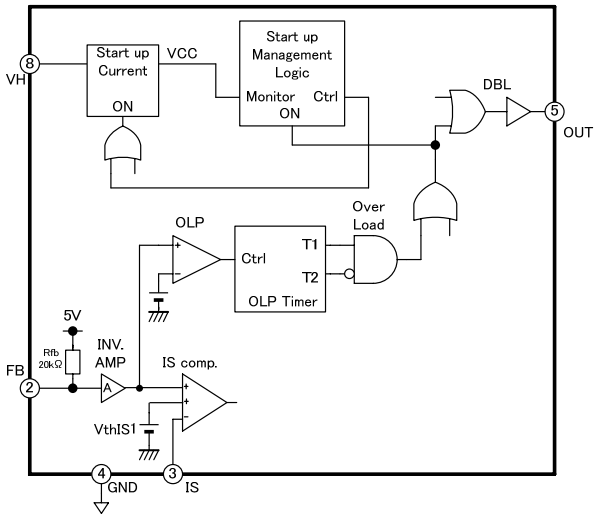


Fig. 11 Overload protection circuit (auto reset type)

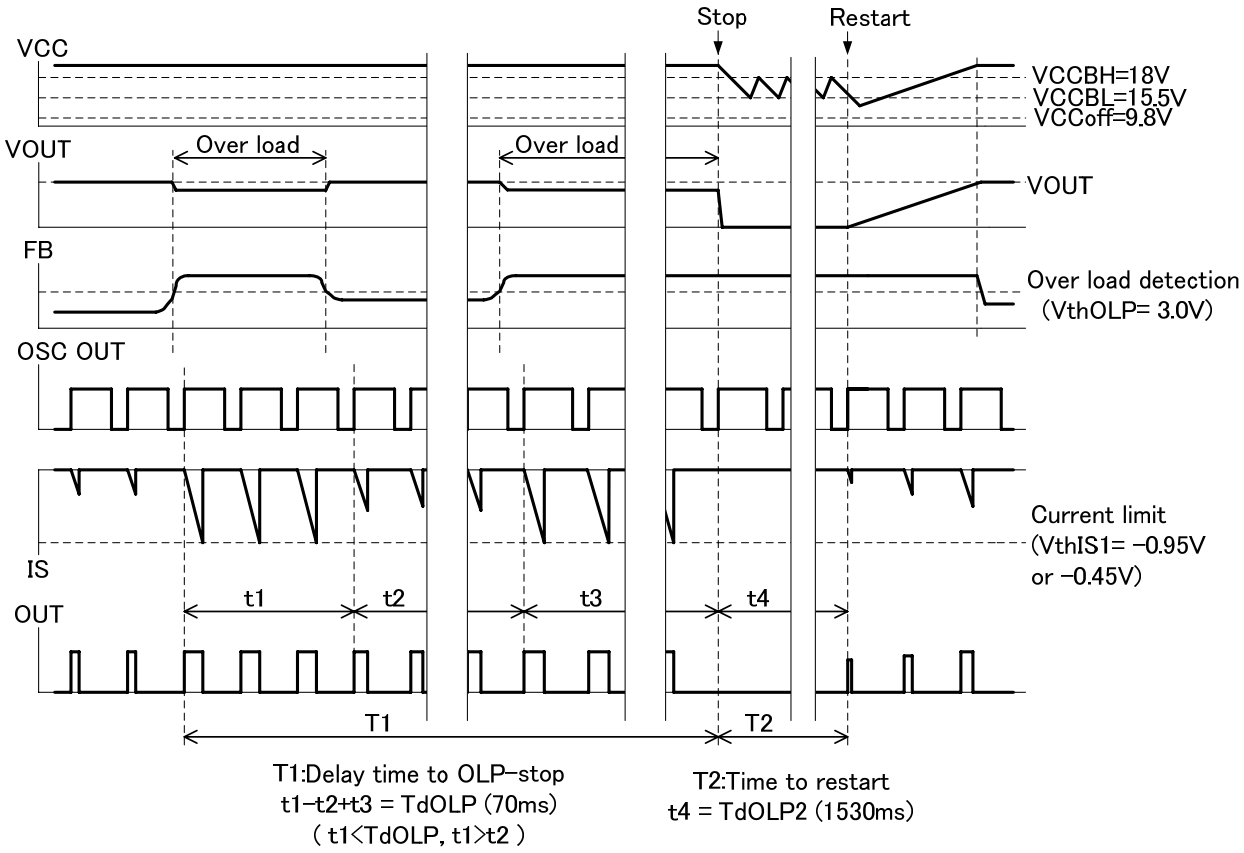


Fig. 12 Overload protection timing chart (auto reset type)

Since the OLP timer for overload protection delay time uses an up/down counter, a period for counting down is required to clear the count. Note that oscillation frequency (Fosc) is counted to detect the overload protection delay time (TdOLP).

Consequently, if overload is reset within the overload protection delay time (less than 70ms), and the switching frequency decreases (down to less than 60kHz or 100kHz) immediately after that, the time for resetting the count is prolonged. In the case of a pulse load with which another overload occurs before the counter is reset, the next overload delay time should be made shorter (70ms or shorter).

Example: In the case of a load with which overload current period of 50ms and no-load period of 1s are repeated, overload protection occurs within the overload delay time (70ms or shorter) as shown in Fig.13. Pay attention to the above in the case of a load with which overload and light load are repeated.

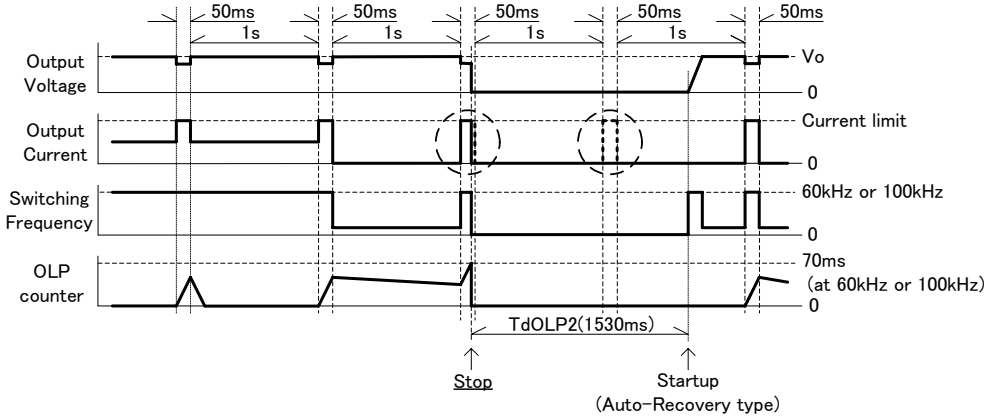


Fig. 13 Typical overload/light load repetition timing chart

(6) Overload protection circuit (latch shutdown type)

Fig.14 shows a latch shutdown type circuit block, and Fig.15 shows the protection operation timing chart.

The latch shutdown type operates on the same principle as the auto reset type up to switching stop.

After the overload protection delay time TdOLP (70ms typ) has elapsed, the switching pulse output is stopped and the latch mode is entered.

After the latch mode is entered, the one-time clamp circuit discharges the VCC voltage rapidly down to 14.5V (typ) (as in the case of the overvoltage protection).

To maintain the latched state in the latch mode, the startup circuit is subjected to the ON/OFF control, and the VCC voltage is maintained within the 12V or 13V (typ) range.

By interrupting the input voltage to decrease the VCC voltage to the OFF threshold voltage (9.8V typ) or lower, the latch mode can be reset.

As described in the section of the auto reset type, in the case of a load with which overload and light load are repeated, latch shutdown may occur within the period of 70ms or shorter.

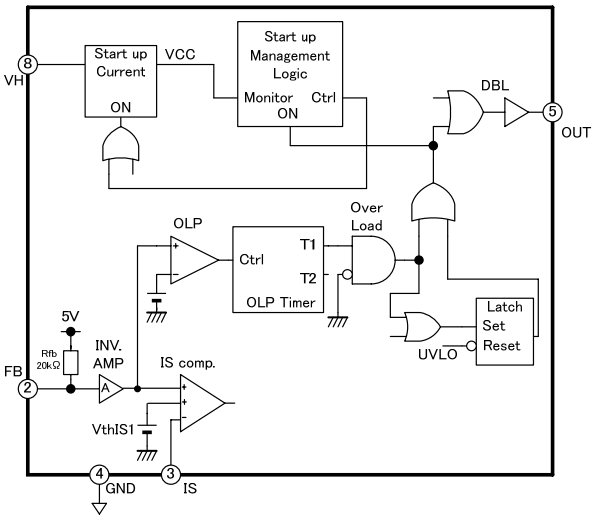


Fig. 14 Overload protection circuit (timer latch type)

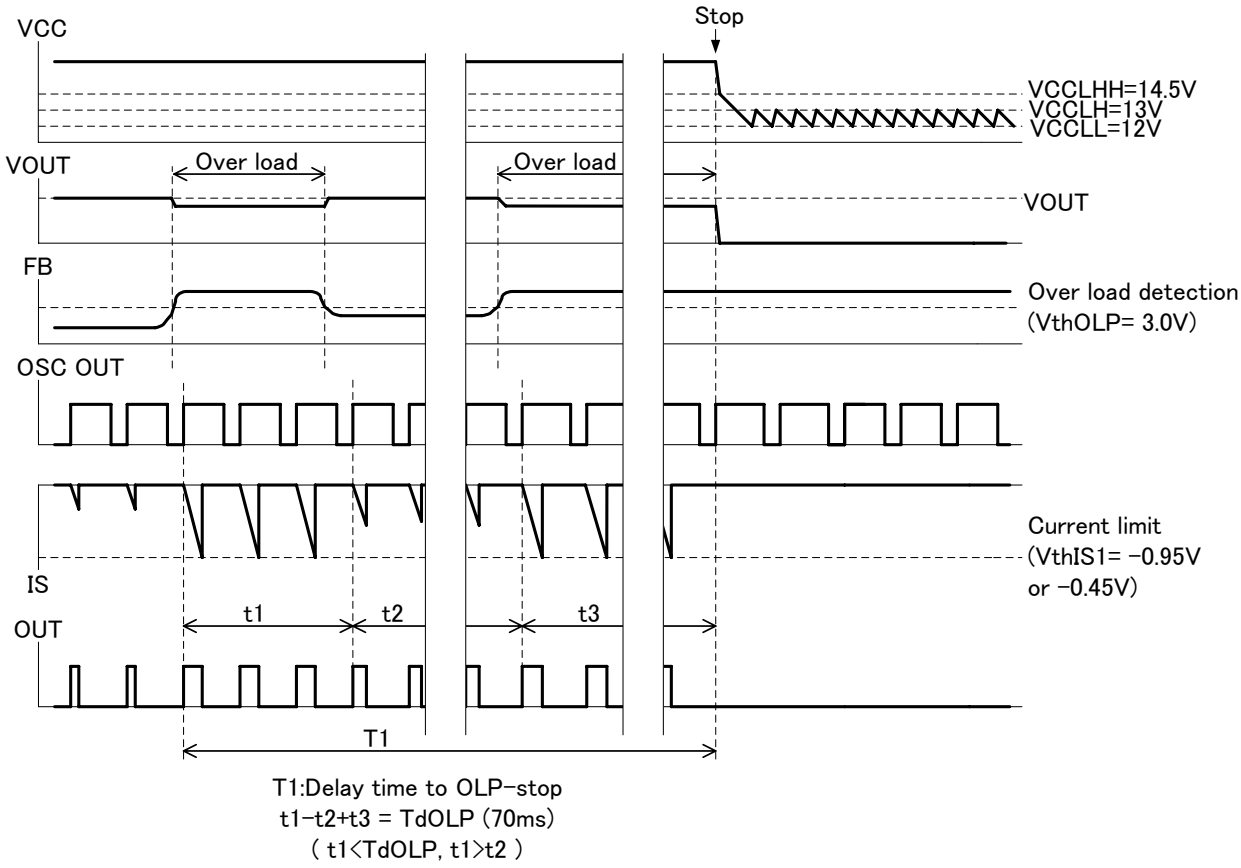


Fig. 15 Overload protection timing chart (timer latch type)

(7) Soft start

The LAT terminal is equipped with a soft start function.
Fig.16 shows the LAT terminal voltage at soft start.

The LAT terminal voltage increases to 2.1V at the time of startup, and then discharged by the constant current source (70uA typ) down to 1.25V. During this period when the LAT terminal voltage decreases from 2.1V to 1.5V, soft start operation is performed.
By adjusting the capacity of the capacitor to be connected to the LAT terminal, the soft start time can be set.
Approximate soft start time can be calculated using the following expression:

$$Tss = (2.1 - 1.5) \times CLAT/70\ \mu A = 0.0086 \times CLAT[\mu F]$$
$$Tss[ms] = 8.6 \times CLAT[\mu F]$$

where, Tss is soft start time.

The maximum recommended value (2.2uF) of the LAT terminal capacity CLAT listed in 6-(2) assumes that the power supply startup time is approximately 20ms. If longer soft start time is set, the value can be increased to approximately 10μF.
The soft start time is affected by a thermistor connected to the LAT terminal for overheat protection, if any.

Even if soft start is not necessary, connect a capacitor to prevent the LAT terminal voltage from decreasing instantaneously down to 1.05V or lower due to constant current discharge for soft start, thus causing latch shutdown to occur.
(See 8-(8) Latch shutdown circuit by an external signal.)

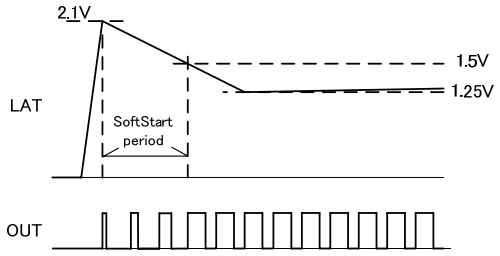


Fig. 16 LAT terminal soft start operation

(8) Latch shutdown circuit by an external signal

The LAT terminal is equipped with a latch shutdown function. (See Fig.17)
By decreasing the LAT terminal voltage to 1.05V or lower, the IC enters the latch mode.
To reset the latch mode, interrupt the input voltage, thus decreasing the VCC voltage to the OFF threshold voltage (9.8V typ) or lower.

If the external latch shutdown function by the LAT terminal is not to be used, connect a capacitor only.

Connect an NTC thermistor to the LAT terminal to use the overheat protective function. (See Fig.17)

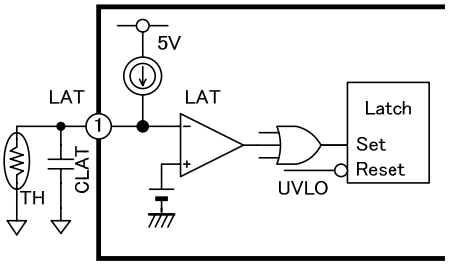


Fig. 17 Overheat protection function using a thermistor

(9) Overvoltage protection circuit (VCC terminal)

The IC integrates an overvoltage protection circuit for monitoring the VCC terminal voltage. (See Fig.18)

If the VCC voltage increases and exceeds 26V typ, which is the reference voltage of the comparator (OVP), the comparator output is reversed to High level, setting the latch circuit to perform latch shutdown.
At this time, the startup circuit is subjected to ON/OFF control to maintain the latch mode, thus keeping the VCC voltage within the 12V or 13V (typ) range.
To reset the latch mode, interrupt the input voltage to decrease the VCC voltage down to the OFF threshold voltage (9.8V typ) or lower.
Since 65μs (typ) delay time has been set to the set input of the latch circuit, the latch mode is not entered even if the VCC terminal exceeds the detection voltage temporarily.

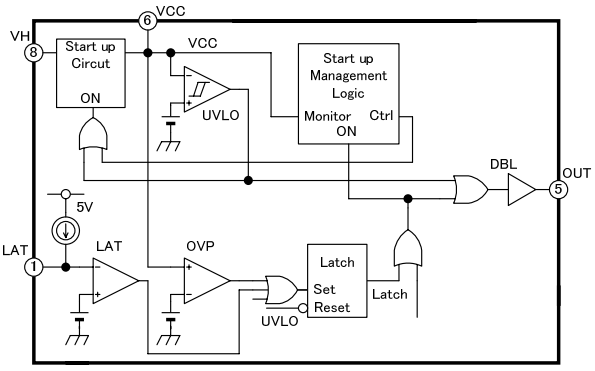


Fig. 18 Overvoltage protection circuit

(10) Undervoltage lockout circuit (VCC terminal)

The IC integrates an undervoltage lockout (UVLO) function to prevent circuit malfunction that might occur when power supply voltage decreases. When the VCC voltage increases from 0V and reaches 18V (typ), the circuit starts operating. When the VCC decreases down to 9.8V (typ), the circuit stops operating.
In a state in which the undervoltage lockout function is actuated to stop IC operation, the OUT terminal is forcibly made to enter the Low state. The latch mode of the protection circuit is also reset.

(11) Output unit

The push/pull structure output circuit drives the MOSFET directly. The peak output current of the OUT terminal is 0.5A (source) and 1.0A (sink) in the maximum absolute ratings.

In a state in which the IC is stopped in the undervoltage lockout circuit or operation is suspended in the latch mode, or in an auto reset wait state by overload protection function, the OUT terminal is brought into the Low level, and the MOSFET is interrupted.

(12) Brown out (low AC input voltage protection)

This IC integrates a brown out function that stops the output pulse of the OUT terminal when the AC input voltage decreases to protect the circuit.

Integration of a high withstand voltage resistor eliminates the need of external parts.

Switching is started when the peak of the AC input voltage to the VH terminal reaches the brown in threshold voltage (104V typ). (See Fig.19)

When the input voltage decreases down to brown out threshold voltage (99V typ) or lower, the output is stopped after 50ms (typ) of delay time. (See Fig.20)

The brown out function is actuated after the UVLO is reset. While switching operation is suspended by the brown out function, the startup circuit is subjected to ON/OFF control to maintain the VCC voltage within the 15.5V to 18V (typ) range.

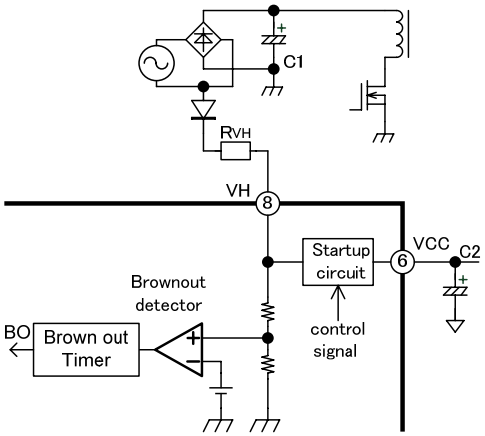


Fig. 19 Brown in and brown out detection circuit

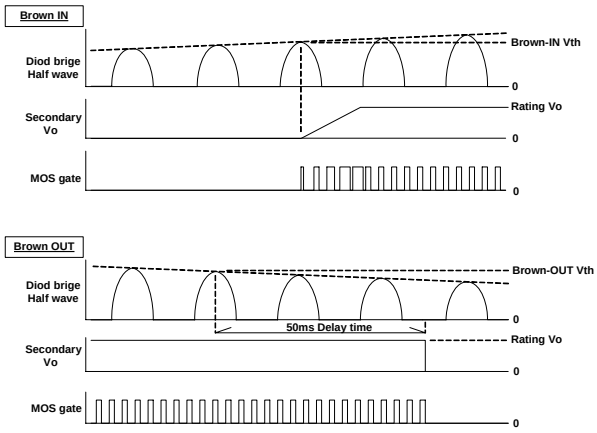


Fig. 20 Conceptual diagram of brown in and brown out operations

9. Advice for designing

(1) Startup

To properly start or stop the power supply, a capacitor having appropriate capacitance must be selected. (See Fig.21)

Fig.22 shows the VCC voltage at the time of startup when an appropriate capacitor is connected.
When the power is turned on, the capacitor of the VCC is charged with the current supplied from the startup circuit, and the voltage increases.
When the VCC reaches the ON threshold voltage, the IC starts operating. The IC is operated based on the voltage supplied from the auxiliary winding. Note that during the period immediately after startup until the voltage of the auxiliary winding starts up, the VCC decreases. Select a capacitor for the VCC that does not allow the VCC to decrease down to the OFF threshold voltage.
Specifically, a VCC terminal capacitor whose OFF threshold voltage is 11V or higher is recommended.

If the capacitance of the VCC terminal is too small, VCC decreases to lower than the OFF threshold voltage before the voltage of the auxiliary winding starts up as shown by Fig.23. In this case, the VCC repeats up/down operation between ON and OFF threshold voltages, and consequently the power supply cannot be turned on.

To prevent the VCC terminal voltage from decreasing to lower than the UVLO OFF threshold voltage due to sudden load change and other reasons, it may be desirable that the capacitance of the capacitor to be connected to the VCC terminal be made larger.
However, if the capacitance of the capacitor of the VCC terminal is increased, the startup time is made longer.
In such cases, the circuit shown in Fig.24 can balance the capacitance and the startup time.
By setting C2 to less than C3, the startup time can be kept short. Since current is supplied via C3 after startup, the VCC terminal voltage hold time can be kept long even under sudden change conditions.

(2) VCC hold time

When the load of the power circuit is short-circuited, power supply from the auxiliary winding is interrupted, causing VCC to decrease. In this case, by resetting the VCC terminal when it decreases to lower than the OFF threshold voltage, VCCoff (9.8V typ), before the overload protection delay time (TdOLP) elapses, startup and stop are repeated. By this operation, the latch type is not stopped by latch shutdown, but run and stop are repeated irrespective of the auto reset wait time TdOLP2 (1530ms typ). (See Fig.25)
To avoid this phenomenon, connect a capacitor whose capacitance does not allow VCC voltage to decrease down to the OFF threshold voltage on occurrence of short circuit of the load of the power circuit.

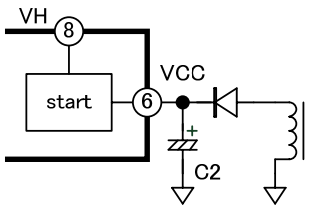


Fig. 21 VCC terminal circuit

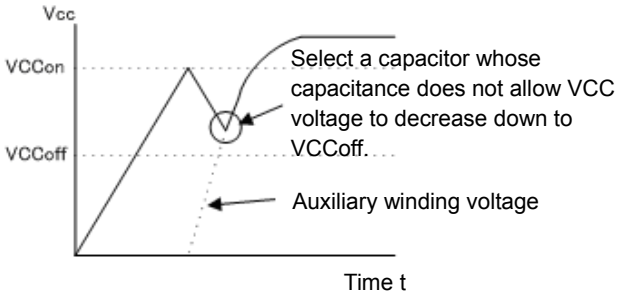


Fig. 22 VCC terminal voltage at startup

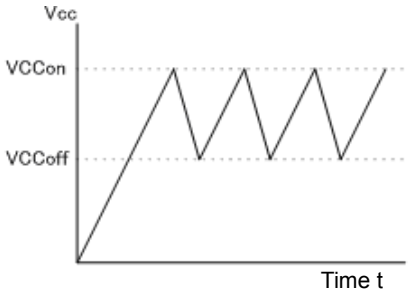


Fig. 23 VCC terminal voltage at startup (when capacitance is too small)

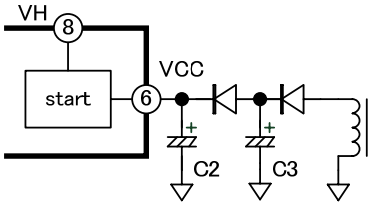


Fig. 24 VCC circuit (shortening of startup time)

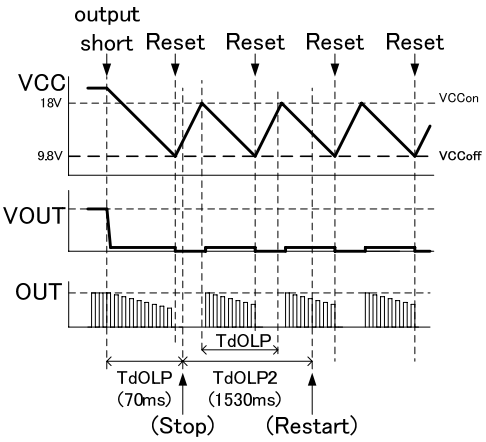


Fig. 25 VCC hold time (at output short circuit)

(3) Gate drive circuit

To adjust switching speed and prevent vibration of the gate terminal, a resistor is connected between the MOSFET gate terminal and the OUT terminal of the IC in general.
In some cases, driving current for turning on the MOSFET and that for turning it off are required to be determined separately.
In this case, connect a gate drive circuit shown in Fig.26 or 27 between the gate terminal of the MOSFET and the OUT terminal.

In Fig.26, the current is limited by R1 and R2 when the power is turned on, while the current is limited only by R2 when it is turned off.
In Fig.27, the current is limited only by R1 when the power is turned on, while the current is limited by R1 and R2 connected in parallel when the power is turned off.

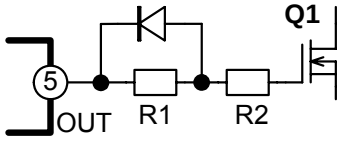


Fig. 26 Gate drive circuit (1)

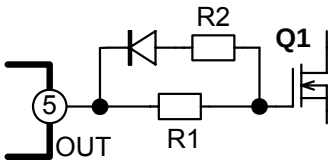


Fig. 27 Gate drive circuit (2)

(4) LAT terminal

• To perform overheat protection using an NTC thermistor

As shown in Fig.17, thermistor TH1 is connected to the LAT terminal to perform overheat protection (latch shutdown).
Since the LAT terminal source current is 60μA (min.), select TH1 whose resistor Rth satisfies the following expression at the desired overheat protection temperature.
If temperature setting for overheat protection is not feasible with TH1 only, connect an additional resistor in series for adjustment.

$$Rth \leq 1.00V / 60\mu A \approx 16.7k\Omega$$

• To perform latch shutdown using an independent abnormality detection signal

To perform latch shutdown with an external signal, connect a peripheral circuit, allowing the LAT terminal voltage to be kept below 1.0V. Fig.28 shows a typical circuit connection.

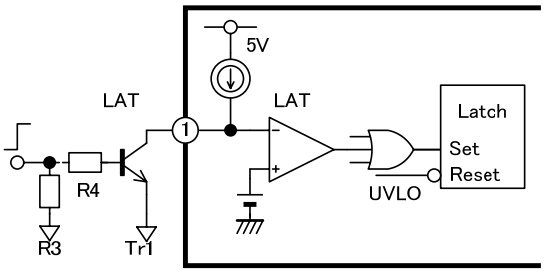


Fig. 28 Latch shutdown function by an external signal

(5) Feedback

Fig.29 shows the circuit configuration of the FB terminal.
A photo-coupler PC is connected as a feedback circuit that monitors the output voltage and performs PWM control.

This signal gives threshold voltage for the current comparator. Consequently, if noise is added to this signal, the output pulses are disturbed. Capacitor C4 is generally connected for protection against noise.

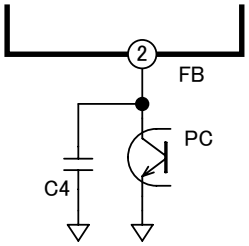


Fig. 29 FB terminal circuit configuration

(6) Current sensing unit

As described in 8-(4) One-shot circuit, the minimum ON width is set for this IC to minimize malfunction due to surge current that occurs when the power MOSFET is turned on.
However, if the surge current that occurs at the time of power ON is large, or noise is applied externally at the time of power ON, malfunction might occur.
In such cases, add RC filters C5 and R7 as shown in Fig.30.
To ensure efficient operation of the capacitor C5, place it as close to the IC as possible, and lay wiring with extreme care.

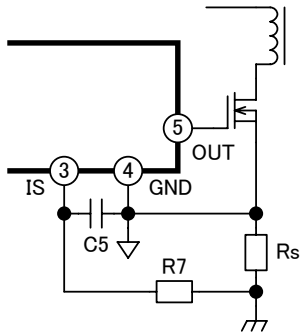


Fig. 30 IS terminal filter

(7) Protection against noise

Since large current is fed to the VCC terminal when the MOSFET is started, relatively large noise is likely to occur. In addition, noise is also generated from the current supplied from the auxiliary winding.
A large noise may cause IC malfunction. To minimize the noise generated at the VCC terminal, connect a bypass capacitor C6 (0.1μF or larger), as shown in Fig.31, adjacent to the VCC terminal of the IC, and between VCC and GND, in addition to the electrolytic capacitor C2.

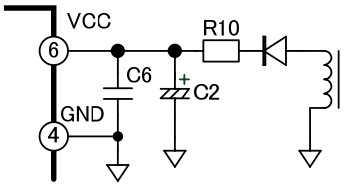


Fig. 31 Noise malfunction prevention (VCC terminal)

If the load is made larger, or due to surge voltage, the VCC voltage increases, actuating the overvoltage protection function. To prevent this phenomenon from occurring, connect resistor R10 (several Ω to several 10Ω) in series with the diode as shown in Fig.31.

(8) Improvement of input power at light load

The IC integrates the function of reducing standby power consumption by lowering oscillation frequency under light load.
However, since load conditions vary depending on the power supply setting, the settings within the IC may be insufficient to reduce standby power consumption.
In such cases, connect resistor R8 as shown in Fig.32 to reduce oscillation frequency.
If R7 is 1kΩ, the resistance of R8 should be approximately several kΩ to 100kΩ. The smaller the R8 value, the lower the switching frequency under light load (positive IS terminal correction).
Also check overload characteristics, which are affected by the correction described above.

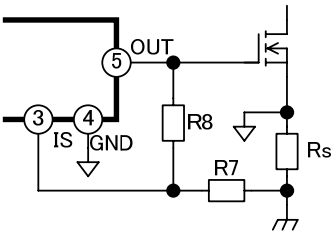


Fig. 32 Correction circuit for improvement of input power under light load

By connecting R8 and C7 in series and connecting them between IS-OUT terminals as shown in Fig.33, the Rs resistance can be set small, allowing the loss to be minimized. Example: R8 = 4.7kΩ, C7 = 100pF

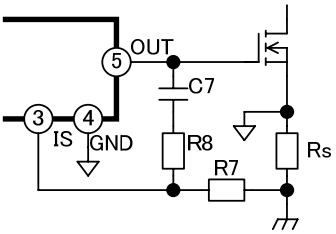


Fig. 33 Correction circuit for improvement of input power under light load

(9) Reduction of dependency of overload detection level on input voltage

Since the gradient of the inductor current of a transformer varies depending on the input voltage in the overload protection function, the current value determined to be overload also varies. The higher the input voltage, the higher the output current that causes overload shutdown to occur.

As shown in Fig.34. resistor R9 can be connected between the auxiliary winding and the IS terminal to minimize the dependency of the overload detection level on input voltage (IS terminal line correction).

If R7 is 1kΩ, the resistance of R9 should be approximately several 10kΩ to several 100kΩ. Note that if the input voltage is made low by correction, the power output current for overload shutdown decreases. Also note that the correction described above affects the input power under light load.

Since the polarity of the detection voltage of the IS terminal is negative, the loss of correction resistance can be lower than that of the positive-polarity system (correction made based on AC rectification voltage).

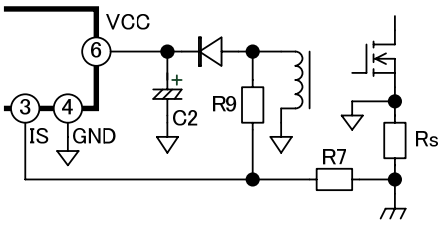


Fig. 34 Reduction of dependency of overload detection level on input voltage

(10) Prevention of malfunction due to negative potential of the terminal

If large negative voltage is applied to each terminal of the IC, the parasitic element within the IC may be actuated, thus causing malfunction to occur. Be sure to maintain the voltage to be applied to each terminal within the maximum absolute ratings.

(11) Loss calculation

To use the IC within its ratings, the loss of the IC may have to be found. However, it is not feasible to measure loss directly. The following is an example of finding a rough value of loss by calculation.

The rough value of the total loss of the IC, Pd, can be calculated using the following expression:

$$Pd \approx VCC \times (ICCop1 + Qg \times fsw) + VVH \times IHrun$$

where,
VVH: voltage to be applied to the VH terminal,
IHrun: current fed to the VH terminal during operation,
VCC: power voltage,
ICCop1: Consumption current of the IC
Qg: electrical charge to be input to the MOSFET gate used, and
Fsw: switching frequency.

A rough value can be found using the above expression, and the total loss found by the calculation, Pd, is slightly larger than the actual value.

Be sure to take into consideration that each characteristic value varies depending on temperatures and other factors.

Example:

When the VH terminal is connected to a half-wave rectifier circuit with 100VAC input, the average voltage to be applied to the VH terminal is calculated to be approximately 45V, and the average current to be fed to the VH terminal is approximately 130 μA;.

Furthermore, assuming that Tj = 25°C, VCC = 18V, and Qg = 80nC, and based on

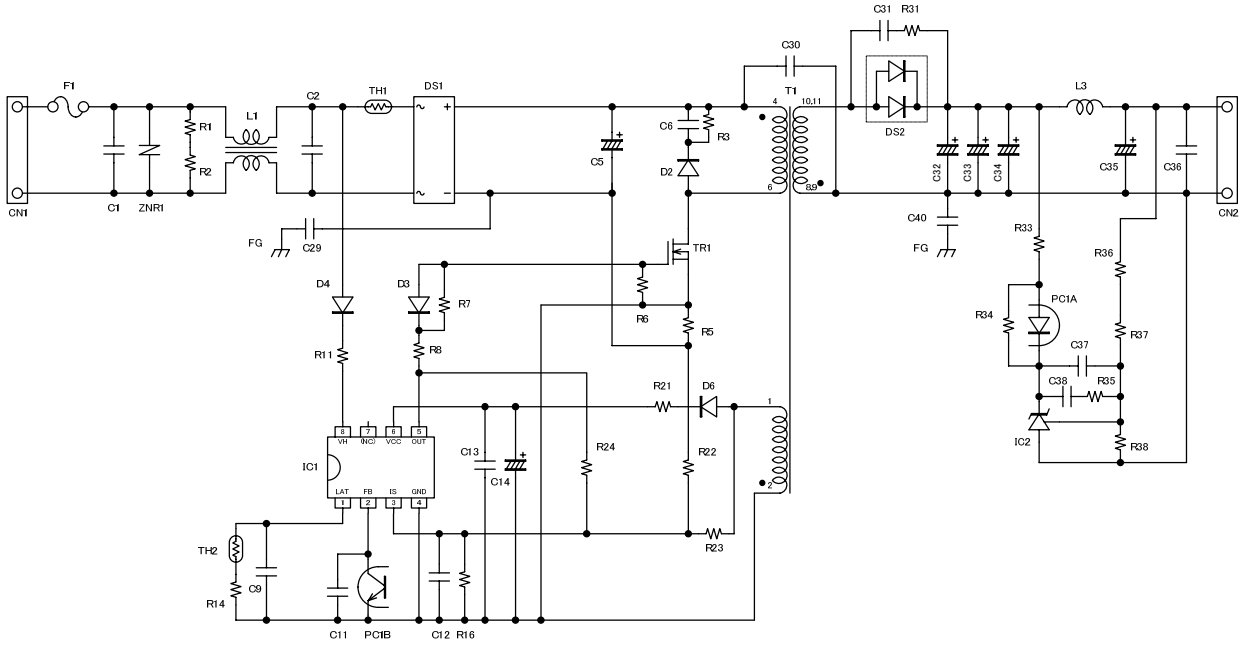
IHrun = 130μA,
ICCop1 = 1.3mA (typ),
and fsw = 60kHz (typ) (product having Fosc = 60kHz),

the loss of the IC having standard characteristics can be calculated as follows:

$$Pd \approx 18V \times (1.3mA + 80nC \times 60kHz) + 45V \times 130\mu A$$
$$\approx 112mW$$

10. Application circuit example

・Vout=19Vdc, Iout=3.6A (Po=68w)　Input voltage=80Vac to 264Vac. (DEMO Board)



Caution

VH Pin is connected to near by diode bridge(DS1) to avoid VH Pin’ s surge voltage it happens by change of startup current when startup circuit repeats on-off operating.

・Part List

Component	Item	Type or Value	Qty
IC1	IC	**FA5558/FA5587 (Fuji)**	1
IC2	IC	TA76431F	1
TR1	FET	**2SK3677-01MR (Fuji)**	1
DS1	diode	D5SBA60	1
DS2	diode	**YG868C15R (Fuji)**	1
D2	diode	EG01C	1
D3,6	diode	**ERA92-02 (Fuji)**	2
D4	diode	D1N60	1
PC1	PhotoCoupler	TLP421F	1
T1	transformer	EER28 (Np : Ns : Nb = 63 : 11 : 9)	1
L1	coil	12mH	1
L3	coil	3.3uH	1
F1	Fuse	3.15A	1
C1	Film capacitor	0.47uF	1
C2	Film capacitor	0.22uF	1
C5	capacitor	220uF	1
C6,40	capacitor	0.01uF	2
C9	capacitor	1uF	1
C11	capacitor	0.01uF	1
C12	capacitor	220pF	1
C13,16	capacitor	0.1uF	2
C14	capacitor	22uF	1
C36,37,38	capacitor	0.1uF	3
C29	capacitor	2200pF	1
C30	capacitor	2200pF	1
C31	capacitor	1500pF	1
C32,33,34,35	capacitor	470uF	4

Component	Item	Type or Value	Qty
R1,2	resistor	1MΩ	2
R3	resistor	47kΩ	1
R5	resistor	0.68Ω	1
R6	resistor	10kΩ	1
R7	resistor	68Ω	1
R8	resistor	10Ω	1
R11	resistor	2.2kΩ	1
R14	resistor	13kΩ	1
R16	resistor	5.1kΩ	1
R21	resistor	2.2Ω	1
R22	resistor	1.2kΩ	1
R23	resistor	360kΩ	1
R24	resistor	33kΩ	1
R31	resistor	10Ω	1
R33	resistor	3.3kΩ	1
R34	resistor	1kΩ	1
R35	resistor	10kΩ	1
R36	resistor	15kΩ	1
R37	resistor	1kΩ	1
R38	resistor	2.4kΩ	1
TH1	Power thermistor	10Ω	1
TH2	thermistor	100kΩ	1
ZNR1	Surge absorber	680V	1

Note)

This application circuit example shows typical directions for use of this IC for reference and does not guarantee the operation and characteristics.

・DEMO Board Typical characteristic curves(FA5558/87)